SHRI ANGALAMMAN COLLEGE OF ENGINEERING

AND TECHNOLOGY

(An ISO 9001:2008 Certified Institution)

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FS 81504

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

EC1201 DIGITAL ELECTRONICS

UNIT – I

***PART-A (2* Marks)**

1) Define binary logic?
2) Convert $(634)_8$ to binary
3) State the different classification of binary codes?
4) Convert 0.640625 decimal numbers to its octal equivalent.
5) State the steps involved in Gray to binary conversion?
6) What is meant by bit & byte?
7) List the different number systems.
8) State the abbreviations of ASCII and EBCDIC code
9) What are the different types of number complements.
10) State the associative property of Boolean algebra.
11) State De Morgan's theorem.
12) Simplify the following using De Morgan's theorem [((AB)'C)'' D]'
13) What is a Karnaugh map?
14) Find the minterms & maxterms of the logical expression :
15) What are called don't care conditions?

PART-B

1. Determine the prime implicants of the function
   F (W,X,Y,Z) = _ m (1,4,6,7,8,9,10,11,15) (16)
2. Simplify the Boolean function using K-map.
   F(A,B,C,D,E) = (0,2,4,6,9,13,21,23,25,29,31) (16)
3. Reduce the following function using K-map technique
   f(A,B,C,D)=_ M (0,2,3,8,9,12,13,15) (16)
4. Reduce the following function using k-map technique

f(A,B,C,D)= _ M(0,3,4,7,8,10,12,14)+d(2,6) (16)

5. Reduce the following function using K-map technique

F(A,B,C,D,E)= _ M(0,4,5,6,7,8,12,15,21,26,27,30)+d(1,9,17,19,25,29). (16)

UNIT – II

PART-A (2 Marks)

1. What are Logic gates?
2. What are the basic digital logic gates?
3. Which gates are called as the universal gates? What are its advantages?
4. Classify the logic family by operation
5. State the classifications of FET devices.
6. Mention the classification of saturated bipolar logic families.
7. Mention the different IC packages.
8. Mention the important characteristics of digital IC's.
9. Define Fan-out & fan in.
10. Define power dissipation.
11. What is propagation delay?
12. Define noise margin.
13. What is Operating temperature?
14. What are the types of TTL logic?
15. State the advantages and disadvantages of TTL

PART-B (16 Marks)

1. Explain with neat diagrams TTL. (16)
2. Discuss all the characteristics of digital IC's. (16)
3. Explain in detail about schottky TTL. (16)
4. Explain with neat diagrams ECL. (16)
5. Explain with necessary diagrams MOS (16)
6. Explain in detail about interfacing CMOS and TTL device (16)
7. Give the comparison between TTL and CMOS families (16)

UNIT III

PART-A (2 Marks)

1. Define combinational logic.
2. Explain the design procedure for combinational circuits.
3. Define decoder & binary decoder.
4. Define Encoder & priority Encoder.

5. Define multiplexer.

6. What do you mean by comparator?

7. Define carry propagation delay.

8. Write the truth table and logic circuit for half adder?

9. Explain the condition for parallel adder/subtractor

10. Draw the logic circuit of full adder using half adder.

11. Explain the carry generate and carry propagate.

12. Define parity generator.

13. Draw the block diagram of multiplexers.

14. Define parity checker

15. Explain even and odd parity

PART-B (16 Marks)

1.Explain the binary division and also explain the Non restoring division and Restoring Division

with Example. (16)

2. Design a logic circuit to convert the BCD code to Excess – 3 codes. (16)

3. Explain the carry look ahead adder (16)

4. Explain the BCD adder with examples (16)

5. Explain the any two code converters (16)

Unit IV

PART-A (2 Marks)

1. What are the classifications of sequential circuits?

2. Define Flip flop.

3. What are the different types of flip-flop?

4. What is the operation of JK flip-flop?_

5. Define race around condition.

6. What is edge-triggered flip-flop?

7. What is a master-slave flip-flop?

8. Define rise time & fall time.

9. Define skew and clock skew.

10. Define setup time.
11. Define hold time.
12. Define register.
13. Define shift registers.
14. What are the different types of shift type?
15. Define synchronous & asynchronous sequential circuit

PART-B (16 Marks)

1. Explain the analysis of clocked sequential circuits with examples (16)
2. Explain the working of BCD Ripple Counter with the help of state diagram and logic diagram.(16)
3. Design an asynchronous sequential circuit with 2 inputs T and C. The output attains a value of 1 when T = 1 & C moves from 1 to 0. Otherwise the output is 0. (16)
4. A asynchronous sequential machine has one input line where 0's and 1's are being incident.The machine has to produce a output of 1 only when exactly two 0's are followed by a '1' or exactly two 1's are followed by a '0'.Using any state assignment and JK flipflop,synthesize the machine (16)
5. Design an asynchronous sequential circuit with 2 inputs X and Y and with one output ZWherever Y is 1, input X is transferred to Z .When Y is 0; the output does not change for anychange in X.Use SR latch for implementation of the circuit (16)
6. Develop the state diagram and primitive flow table for a logic system that has 2 inputs, x and y and an output z. And reduce primitive flow table. The behavior of the circuit is stated as follows. Initially x=y=0. Whenever x=1 and y = 0 then z=1, whenever x = 0 and y = 1 then z = 0.When x=y=0 or x=y=1 no change in z ot remains in the previous state. The logic system has edge triggered inputs with out having a clock .the logic system changes state on the rising edges of the 2 inputs. Static input values are not to have any effect in changing the Z output (16)
7. Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 1, input X is transferred to Z. When Y is 0,the output does not change for any change in X. (16)
8. Obtain the primitive flow table for an asynchronous circuit that has two inputs x,y and one output Z. An output z =1 is to occur only during the input state xy = 01 and then if

the only if the input state xy =01 is preceded by the input sequence. (16)

9. Draw the state diagram and characteristics equation of T FF, D FF and JK FF
10. Design and explain the working of a synchronous mod – 7 counter (16)
11. Design and explain the working of a synchronous mod –3 counter (16)
12. Explain in detail about shift register. (16)

UNIT V

PART-A (2 Marks)

1. What are the types of ROM?
2. Explain PROM.
3. Explain EPROM.
4. Explain EEPROM.
5. What is programmable logic array? How it differs from ROM?
6. Give the classification of PLDs.
7. Define PLA
8. Define PAL
9. Why was PAL developed ?
10. Define GAL
11. What is CPLD ?
12. What is Read and Write operation?
13. Define Static RAM and dynamic RAM
14. Define Cache memory
15. Give the feature of flash memory.

PART – B

1. Explain in detail about PLA with a specific example. (16)
2. Explain with neat diagrams RAM architecture. (16)
3. Explain in detail about PLA and PAL. (16)
4. Explain with neat diagrams a ROM architecture. (16)
5. Explain in detail about RAM organization (16)
6. Explain the static RAM and dynamic RAM. (16)
7. Explain and draw the memory cycles and timing waveforms (16)
8. Details briefly about Field programmable gate arrays (16)

9. Explain in detail about memory decoding (16)